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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/053,431	01/17/2002	Chris Yoochang Chung	UNIV0123	3518

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EXAMINER	
NGUYEN, HAU H	

ART UNIT	PAPER NUMBER
2676	2

DATE MAILED: 11/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/053,431	CHUNG ET AL.	
	Examiner	Art Unit	
	Hau H Nguyen	2676	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-2, 11-24, 26-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Van Hook et al. (U.S. Patent No. 6,342,892).

Referring to claims 1, 16, 23-24, 27-28, Van Hook et al. teach a graphics pipeline comprising a signal processor 400 as shown in Fig. 6. As shown in Fig. 7, the signal processor 400 includes an instruction memory 402 (instruction cache) for storing microcode for execution by vector unit 420, a plurality of register files 422 (0)-422(7), a vector processing unit 420, which comprises eight 16-bit calculating elements capable of performing numerical calculations in parallel. Vector unit 420 is especially suited for graphics matrix calculations and certain kinds of digital audio signal processing operations (col.15, lines 60-67, and col. 16, lines 1-11). Van Hook et al. further teach the graphics data may be of variable size (col. 36, lines 12-15).

In regard to claim 2, Van Hook et al. teach a texture memory 502 in communication with the vector processing unit through the signal processor 400 as shown in Fig. 6.

Referring to claims 11, 12, 15, and 29, FIG. 7A shows an example of a register instruction format 450 and how signal processor 400 uses that register instruction format to access three 128-bit wide words 452 within data memory 404. Register instruction format 450

may include a 6-bit operation code field 450(a), a 5-bit source register specifier 450(b), a 5-bit target (source/destination) register specifier 450(c), a 5-bit destination register specifier 450(d), and a parameter field 450(e). As shown in FIG. 7B, Van Hook et al. teach vector unit 420 treats each of these 128-bit words as a concatenated sequence of eight 16-bit values (output buffer), and operates on each of the 16-bit values in parallel (col. 18, lines 37-54) (partitioned data).

In regard to claims 13 and 14, as shown in Fig. 6, Van Hook et al. teach a memory interface 512 (write buffer) coupled to a blender 510 for performing read, modify and write operations for the individual pixels, and also has special modes for loading/copying texture memory 502, filling rectangles (fast clears), and copying multiple pixels from the texture memory 502 into the frame buffer 118. Memory interface 512 has one or more pixel caches to reduce the number of accesses to main memory 300 (col. 16, lines 31-37).

Referring to claims 17, and 21-22, as cited above, Van Hook et al. shows in Fig. 7B an example slicing of the instruction format for processing by the vector unit. As shown in Fig. 3, the signal processor not only perform graphics commands, but also sound (media) commands. As also shown in Fig. 3, data after being processed is stored in main memory 128 and 132.

In regard to claims 18-20, as cited above, Van Hook et al. teach the register instruction format 450 (Fig. 7A) includes a 5-bit destination register 450(d). Van Hook et al. further teach the texture unit can apply texture maps stored within texture memory 502 onto textured areas defined by primitive edge equations solved by rasterizer 504. The color combiner 508 combines and interpolates between the texture color and a color associated with the graphic primitive (col., lines 22-26).

Referring to claim 26, as cited above, Van Hook et al. teach a blending unit, an output buffer, and a write buffer.

In regard to claim 30, as cited above, Van Hook et al. teach a graphics pipeline for processing data of variable length comprising a vector processing unit for generating pixel coordinate to the display processor, and a data memory 404 for storing input data (caching) (Fig. 6). When a word in data memory 404 is retrieved for use by vector unit 420, it is sliced into eight 16-bit segments, with each segment being sent to a different register file 422 within vector unit 420 (see FIG. 7B, and col. 19, lines 15-20). Van Hook et al. further teach the signal processor comprise a microcode RAM 402 for mapping addresses to address space of the main processor 100 (col. 12, lines 5-14).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3-10, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Hook et al. (U.S. Patent No. 6,342,892) in view of Gossett (U.S. Patent No. 6,104,415).

Referring to claims 3-4, and 25, as shown in Fig. 6, Van Hook teach a rasterizer 504. Thus,Van Hook et al. teach all the limitations of claims 3,4, and 25, except that the texture cache includes a line buffer and cache areas, the graphics pipeline further includes a texture address unit in communication with the texture cache.

However, Gossett teaches a graphics pipeline comprising a texture cache 74 coupled to a texture address unit 68 as shown in Fig. 5. As shown in FIG. 10, texture cache 74 comprises table 75 and memory 87. Memory 87 stores the data associated with the texture cache 74, which is texel values (cache areas). Table 75 stores a mapping relationship between the texel numbers indicated by the texel address 72 to the SDRAM addresses (line buffer) (col. 16, lines 16-21).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Gossett in combination with the method as taught by Van Hook et al. in order to accelerate minified texture cache access of the computer graphics hardware (col. 1, lines 26-30).

In regard to claim 5, although Van Hook et al. do not teach the texture address unit generate filter coefficients, Gossett teaches the texture address unit 68 outputs a set of quad texel addresses 72 which are applied to the texture cache 74 so that a corresponding and proper set of texel fragments are retrieved from the texture cache 74 for eventual filtering (col. 11, lines 60-66).

Therefore, it would have been obvious to one skilled in the art to utilize the method as taught by Gossett in combination with the method as taught by Van Hook et al. in order to accelerate minified texture cache access of the computer graphics hardware (col. 1, lines 26-30).

Referring to claims 6-10, as shown in Fig. 6, Van Hook et al. teach the graphics pipeline includes a rasterizer 504, a color combiner 508, and a blender 510. Rasterizer 504 rasterizes polygon (e.g., triangle, and rectangle) geometric primitives to determine which pixels on the display screen 60 are within these primitives. The color combiner 508 combines and interpolates between the texture color and a color associated with the graphic primitive. Blender 510 blends

the resulting pixels with pixels in frame buffer 118, and is also involved in performing Z buffering (i.e., for hidden surface removal and anti-aliasing operations) (col. 16, lines 16-31).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hau H. Nguyen whose telephone number is: 703-305-4104. The examiner can normally be reached on MON-FRI from 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on 703-308-6829.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D. C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered response should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

H. Nguyen

10/30/2003

Matthew C. Bella

MATTHEW C. BELLA
SUPERVISORY PATENT EXAMINER
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